WE CLAIM:

1. A semiconductor manufacturing process for forming the active region of a Silicon-On-Insulator (SOI) device comprising the steps of:

providing a bulk substrate having a buried oxide layer thereon and having a thin undoped SOI silicon layer atop said buried oxide layer;

depositing a polysilicon layer atop said SOI silicon layer and patterning a gate feature out of said polysilicon layer, said SOI silicon layer having a top surface, said gate feature having sidewalls and a top and bottom surface, said top surface of said gate feature being further distant from said SOI silicon layer than said bottom surface of said gate feature;

forming dielectric sidewall spacers abutting said gate feature sidewalls;

etching through said top surface of said gate feature to form a first and a second tapered polysilicon feature, each said first and second tapered polysilicon feature having a base and a top, said bases being wider than said tops, each said tapered polysilicon feature having a tapered surface connecting said base to said top opposite said abutting dielectric sidewall spacers, said first and second tapered polysilicon features having a gap therebetween, said gap having a bottom edge, said bottom edge of said gap being a portion of said top surface of said SOI silicon layer and said bottom edge of said gap having a length;

depositing a gate dielectric onto said bottom edge of said gap and onto said tapered surfaces of said tapered polysilicon features; and

depositing metal onto said gate dielectric to fill said gap.

2. The semiconductor manufacturing method of claim 1, wherein said length of said bottom edge of said gap is less than 50 nm.

3. The semiconductor manufacturing method of claim 2, further including the steps of:

before said step of depositing said polysilicon layer, forming a temporary gate dielectric layer atop said SOI silicon layer;

after depositing said polysilicon layer and prior to patterning said gate feature, depositing a layer of SiON atop said polysilicon layer, said patterned gate feature thereby having a layer of SiON atop said polysilicon, said SiON layer having a top surface;

after said step of patterning said gate feature and prior to said step of forming said dielectric sidewall spacers, implanting extension regions in said SOI silicon layer and annealing said implanted extension regions;

said step of forming dielectric sidewall spacers removing a portion of said temporary gate dielectric not below said gate feature;

after said step of forming dielectric sidewall spacers, implanting source/drain regions in said SOI silicon layer and annealing said implanted source/drain regions;

after said step of implanting said source/drain regions, forming a silicide layer on exposed regions of said SOI silicon layer;

after said step of forming a silicide layer, depositing a layer of TEOS and polishing said TEOS layer to said top surface of said SiON layer; and wherein

said step of depositing said gate dielectric and said step of depositing said metal onto said gate dielectric are performed at temperatures below 800 C.

4. The semiconductor manufacturing process of claim 2, wherein:

said step of etching through said gate feature to form said tapered polysilicon features is performed by Reactive Ion Etching utilizing a mixture of HBr and Cl_2 etch gases;

said step of depositing said gate dielectric comprises Remote Plasma Processing;

said step of depositing said metal onto said gate dielectric is performed using a method selected from the group consisting of: CVD, PVD, electroplating, and Atomic Layer Deposition.

5. A semiconductor manufacturing process for forming the active region of a SOI device comprising the steps of:

providing a bulk substrate having a top surface and having a buried oxide layer and a thin undoped SOI silicon layer thereon, said buried oxide layer having a thickness in the range between 50 and 60 nm, and said SOI silicon layer having a thickness in the range between 5 and 20 nm;

growing or depositing a temporary gate dielectric layer atop said SOI silicon layer, said temporary gate dielectric layer having an equivalent oxide thickness in the range between 0.6 and 2.0 nm;

depositing a layer of polysilicon atop said temporary gate dielectric layer, said polysilicon layer having a thickness in the range between 75 and 100 nm;

depositing a layer of SiON atop said polysilicon layer, said SiON layer having a top surface and having a thickness in the range between 20 and 36 nm, said polysilicon layer and said SiON layer forming a polysilicon/SiON stack;

patterning and etching said polysilicon/SiON stack to form a gate feature, said gate feature having a length in the range between 40 and 75 nm, said gate feature having sidewalls;

implanting extension implanted regions;

annealing by RTA for 5 – 10 seconds at a temperature in the range between 900 and 950 C;

depositing a dielectric layer comprising silicon nitride, said dielectric layer having a thickness in the range between 70 – 90 nm;

performing an anisotropic dielectric etch to form dielectric spacers abutting said gate feature sidewalls, said anisotropic dielectric etch removing a portion of said temporary gate dielectric not below said gate feature;

implanting source/drain implanted regions, said gate feature being doped during said source/drain implanting;

annealing by RTA for 5 – 10 seconds at a temperature in the range between 950 and 1025 C;

growing a selective epi silicon layer atop a portion of said SOI silicon layer not below said gate feature, said selective epi silicon layer having a thickness in the range between 20 and 25 nm;

depositing a cobalt layer, said cobalt layer having a thickness in the range between 10 and 12 nm;

annealing said wafer to react a first portion of said cobalt layer with said selective epi silicon layer to convert said selective epi silicon layer to cobalt silicide;

etching away a second portion of said cobalt layer not reacted with said selective epi silicon layer;

depositing a TEOS layer, said TEOS layer having a thickness in the range between 150 and 200 nm;

polishing back said TEOS layer to said top surface of said SiON layer;

installing said wafer in an oxide RIE machine;

etching through said SiON layer to remove said SiON layer, said TEOS layer and said dielectric spacers remaining substantially unaffected by said etching through said SiON layer;

installing said wafer on a wafer chuck in a poly RIE machine having adjustable wafer chuck temperature and adjustable gas flows;

flowing a mixture of gases including Cl_2 and HBr;

performing RIE poly etch to etch through said gate feature to form a first and a second tapered polysilicon feature, said first and second tapered polysilicon features having bases and tops, said bases being wider than said tops, said tapered polysilicon features additionally having tapered surfaces opposite said abutting dielectric sidewall spacers, said tapered surfaces being at an angle with respect to said top surface of said bulk substrate, said first and second tapered polysilicon features having a gap therebetween, said gap having a bottom edge, said bottom edge of said gap being a portion of said top surface of said SOI silicon layer; said bottom edge of said gap having a length, said RIE poly etch stopping on said temporary dielectric layer, a portion of said temporary dielectric layer remaining after said RIE poly etch;

performing a wet etch to remove said portion of said temporary dielectric layer remaining after said RIE poly etch;

performing a wet etch in a mixture of NH_4OH and H_2O_2 to remove about 30 Angstroms of said SOI silicon layer at said bottom edge of said gap;

installing said wafer in a Remote Plasma Processing machine;

depositing a final gate dielectric onto said bottom edge of said gap and onto said tapered surfaces of said tapered polysilicon features, said final gate dielectric having an equivalent silicon dioxide thickness in the range between 1.0 and 1.5 nm, said depositing of said final gate dielectric being at a temperature below 800C;

annealing said wafer at a temperature of about 800C for a time in the range between 1 and 3 minutes;

depositing a layer of metal into said gap and onto said TEOS layer, said depositing of said layer of metal being performed at a temperature below 800C,

said metal being selected from the group consisting of: CVD TiN, CVD W, PVD Al, CVD Al, electroplated Co, electroplated CoWP, electroplated CoWB, electroplated Cr or its alloys, CVD Ni, electroplated Ni, electroplated Pd, electroplated SnPd, Atomic Layer Deposited RuO_2 electroplated Cu or its alloys, electroplated Ag or its alloys, and electroplated Ir and alloys;

polishing said layer of metal off of said TEOS layer by CMP; and

performing a wet etch to remove a portion of said final gate dielectric proximal said tops of said tapered polysilicon features.

6. The semiconductor manufacturing process of claim 5, wherein:

said step of performing RIE poly etch to etch through said polysilicon gate feature to form a first and a second tapered polysilicon feature includes adjusting said wafer chuck temperature within the range of 30 – 70 C and adjusting said Cl_2 and HBr gas flows such that the ratio of Cl_2/HBr flow is in the range between 0.5 and 1.5 , to provide between 10 and 20 nm of polysilicon at said bases of said tapered polysilicon features, said angle of said tapered surfaces being in the range between 75 and 85 degrees; and wherein

said length of bottom edge of said gap is less than 50 nm.

7. An FDSOI device having an active region, said active region being formed by the process of claim 2.

8. An FDSOI device having an active region, said active region being formed by the process of claim 6.

9. An FDSOI device comprising:

a bulk semiconductor substrate having a top surface, a buried oxide layer atop said top surface of said substrate and a thin undoped SOI silicon layer atop said buried oxide layer thereon, said buried oxide layer having a thickness in the range between 50 and 60 nm, and said SOI silicon layer having a top surface and having a thickness in the range between 5 and 20 nm;

a doped gate poly feature on said top surface of said SOI silicon layer, said doped gate poly feature having a length in the range between 40 and 75 nm, said doped gate poly feature having outer sidewalls, said doped gate poly feature comprising a first and a second tapered polysilicon feature having a gap therebetween, said first and second tapered polysilicon features each having a base and a top, each said base being wider than said top, each said tapered polysilicon feature having a tapered surface connecting said base to said top opposite said outer sidewalls, said tapered surfaces being at an angle with respect to said top surface of said bulk substrate, said gap having a bottom edge, said bottom edge of said gap being a portion of said top surface of said SOI silicon layer and said bottom edge of said gap having a length;

said doped gate poly feature has a pair of extension implanted regions in said SOI silicon layer, said extension implanted regions extending under said first and second tapered polysilicon features;

said doped gate poly feature has a pair of dielectric spacers abutting said gate poly feature outer sidewalls, said dielectric spacers having a top and a bottom; and

source/drain implanted regions in said SOI silicon layer, said source/drain implanted regions extending under said dielectric spacers.

10. The device of claim 9 further comprising:

a layer of cobalt silicide atop a portion of said SOI silicon layer not under said gate poly feature or said dielectric spacers; and

a TEOS layer atop said cobalt silicide layer, said TEOS layer having a thickness in the range between 150 and 200 nm, said TEOS layer having a top surface, said top surface of said TEOS layer being substantially even with said top of said dielectric spacers.

11. The device of claim 10 further comprising:

a gate dielectric on said bottom edge of said gap and on a first portion of said tapered surfaces of said tapered polysilicon features, said first portion of said tapered surfaces of said tapered polysilicon features extending at least halfway up said tapered surfaces of said tapered polysilicon features, a second remaining portion of said tapered surfaces of said tapered polysilicon features not having gate dielectric thereon, said gate dielectric having an equivalent silicon dioxide thickness in the range between 1.0 and 1.5 nm, said gate dielectric filling a first portion of said gap between said tapered polysilicon features, a second portion of said gap between said tapered polysilicon features comprising a region abutting said second remaining portion of said tapered surfaces of said tapered polysilicon features not having gate dielectric thereon, said second portion of said gap having a thickness in the range between 1.0 and 1.5 nm; and

a metal gate feature filling a third remaining portion of said gap between said tapered polysilicon features, said metal gate feature being composed of a metal selected from the group consisting of: CVD TiN, CVD W, PVD Al, CVD Al, electroplated Co, electroplated CoWP, electroplated CoWB, electroplated Cr or its alloys, CVD Ni, electroplated Ni, electroplated Pd, electroplated SnPd, Atomic Layer Deposited RuO_2 electroplated Cu or its alloys, electroplated Ag or its alloys, and electroplated Ir and alloys.

12. The FDSOI device of claim 9, wherein said length of said bottom edge of said gap is less than 50 nm, and where said angle of said tapered surfaces of said tapered polysilicon features with respect to said top surface of said bulk substrate is in the range between 75 and 85 degrees.